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ed amargaid nu rajubid nis omitp³Ã o±Ãesid le arap sedadilibisop sairav etnemadip¡Ãr raborp y sacig³Ãlopot senoicatimil sal ed n³Ãisnerpmoc aneub anu renet edeup roda±Ãesid le ,olap ed samargaid sol ed aduya al noC .onarpmet o±Ãesid ed sesaf sal ne o±Ãesid led lareneg aÃgolopot al racifilpmis arap avitcefe yum arenam ed rasu nedeup es euq ,olap ed samargaid ed otpecnoc le someratneserp ,s¡ÃmedA .senoisnemid sal ne y aracs¡Ãm al ed arutcurtse al ne o±Ãesid ed salger sairav ed aicneulfni al rartsom arap ,osap a osap ¡Ãratneserp es elpmis SOMC rosrevni nu ed o±Ãesid lE .atelpmoc o±Ãesid ed salger ed otnujnoc nu ed n³Ãisiver al noc olutÃpac etse someraznemoc ,otnat ol rop ,2 olut-ÃpaC le ne ebircsed es omoc o±Ãesid ed o±Ãesid ed salger ed otnujnoc nu a etnematcirtse esratsuja nebed aracs¡Ãm ed o±Ãesid ed sojubid soL .acisÃf aracs¡Ãm ed o±Ãesid ed osecorp led n³Ãisnerpmoc aneub anu renet ebed n©Ãibmat ISLV ed roda±Ãesid le ,sacisÃf senoicatimil y senoicatimil sal ragzuj arap ,ograbme niS .selatigid ISLV sotiucric sol ed aÃroyam al ed o±Ãesid le arap ereiferp es etnemlareneg)arodatupmoc rop soditsisa otneimaturne y n³Ãicacoloc + radn¡Ãtse sadlec ,olpmeje rop(adazitamotua o±Ãesid ed n³Ãicareneg al ,otnat ol roP .sahcertse yum senoicatimil ojab esrazimitpo ebed otiucric led otneimidner le o/y aer¡Ã le ednod selaicepse saicnatsnucric ne olos elbacifitsuj se euq ,otnel y ovisnetni yum o±Ãesid ed ozreufse nu ereiuqer sacig³Ãl satreup sal ed odallated aracs¡Ãm ed o±Ãesid le ,odal orto roP .n³Ãicnuf atreic nu arap asu es euq oicilis ed aer¡Ã le ,etnemaivbo y ,satis¡Ãrap saicnetsiser y saicnaticapac sal ,serotsisnart sol ed saicnatcudnocsnart sal etnematcerid animreted acisÃf arutcurtse al euq ay)aicnetop ed n³Ãicapisid ,dadicolev ,aer¡Ã(otiucric led lareneg otneimidner la odalucniv etnemahcertse yum ¡Ãtse ocisÃf o±Ãesid led o±Ãesid lE .SOMC ed sacig³Ãl satreup sal arap aracs¡Ãm ed o±Ãesid ed o±Ãesid ed sacis¡Ãb satuap sal n¡Ãratneserp es ,olutÃpac etse nE n³ÃiccudortnI 1.3 complete. the physical design (mask design) of the logical gates of cmos is an iterative process that begins with the topology of the circuit (to realize the desired logical function) and the initial serotsisnart sol ed)L/W(soitar sal ne etnemlareneg nartnecnoc es o±Ãesid ed senoicacifidom saL .esriteper ebed osecorp le odot y odacifidom res ebed o±Ãesid le ,sadaesed senoicacificepse sal noc nedicnioc on)aicnetop ed n³Ãicapisid o soirotisnart atseupser ed sopmeit ,olpmeje rop(odalumis otiucric led otneimidner le iS .adÃartxe aten atsil al odnazilitu ,ECIPS n³Ãicalumis anu odnazilaer ranimreted edeup es otiucric led laer otneimidner le ,arohA .n³Ãiccartxe ed atneimarreh al rop etnemacit¡Ãmotua areneg es euq ,ECIPS adartne ed ovihcrA .ateuqam anu ed n³Ãiccudorp al arap o±Ãesid ed ojulf ocipÃt lE :1.3-adallated arugiF anu etnemlareneg se n³Ãiccartxe ed osap led odatluser lE .odon adac ne sairatisarap saicnaticapac sal ,etnatropmi s¡Ãm y ,selaer rotsisnart ed so±Ãamat sol ranimreted arap odanimret o±Ãesid le ne sotiucric ed n³Ãiccartxe ed otneimidecorp nu azilaer es ,)kcehC eluR ngiseD(lanif CRD le odneiugiS .etnemavitacifingis yum raibmac ebed on acis¡Ãb aÃgolopot al orep ,o±Ãesid ed salger sal sadot radomoca arap senoicareti sa±Ãeuqep sairav rireuqer edeup otneimidecorp etsE .o±Ãesid ed o±Ãesid ed salger sal noc odreuca ed)o±Ãesid ed rotide atneimarreh anu odnazilitu(najubid es aracs¡Ãm ed sapac sal ,elbitcaf etnemacig³Ãlopot o±Ãesid nu rartnocne ed s©ÃupseD .sotcatnoc sol ed senoicacibu sal y serotsisnart sol ed senoicacibu sal odnartsom ,solap ed amargaid ed elpmis o±Ãesid nu rajubid edeup es arohA .serotsisnart sol ed omitp³Ã nedro le ranimreted roda±Ãesid la netimrep htap-reluE odot©Ãm le y ocif¡Ãrg led acig³Ãlopot n³Ãicatneserper al ,serotsisnart 6-4 ed s¡Ãm eneitnoc acig³Ãl atreupmoc al iS .n³Ãixenocretni ed saenÃl sal ed adarepse dutignol al y sovitisopsid ed orem⁰Ãn le ,rodalitnev le ne odasab ,adilas ed odon le ne latot airatisarap agrac al ramitse edeup ol³Ãs roda±Ãesid le ,otnup etse nE .)sadaesed otneimidner ed senoicacificepse sal razilaer arap(serotsisnart sol ed of the transistor), since the proportions of width to the length of the transistors determine the transconductance of the device and the capacitances of parasitic source/drain. The design also can decide to decide ed sedadilibisop sahcum netsixe euq somerev ,ograbme niS .elpmis etnemavitaler se o±Ãesid ed a-Ãgolopot al euq aÃrimusa onu ,otnat ol rop ,SOMP rotsisnart nu y SOMN nu ed atsnoc otiucric lE .osap a osap ¡Ãranimaxe es SOMC rosrevni nu ed aracs¡Ãm ed o±Ãesid ed o±Ãesid le ,n³Ãicaunitnoc A SOMC rosrevni led o±Ãesid ed o±ÃesiD 3.3 .SOMC o±Ãesid ed o±Ãesid ed salger sal ed n³ÃicartsuII :2.3 arugiF .sacin³Ãrcimbus SOMC saÃgoloncet sal arap selit⁰Ã nos on etnemelpmis adbmaL ne sadasab o±Ãesid ed salger sal ,otnat ol roP .savitacifingis saicnerefid netsixe euq artseum adbmaL ne sadasab salger sal noc elpmis n³Ãicarapmoc anU .selaer sarcim ed senoisnemid ne savitatneserper salger ed otnujnoc nu ad es ednod ,ahcered anmuloc al ne artsuli es ohceh etsE .sanorcimbus sa-Ãgoloncet sal arap etnemlaicepse ,etnemlaenil alacse es on salger sal ed aÃroyam al ,sacis¡Ãb senoicatimil sal raziromem arap y aÃgoloncet al ed etneidnepedni aracs¡Ãm ed o±Ãesid nu rinifed arap etneinevnoc yum se selbalacse o±Ãesid ed salger ed otpecnoc le neib is euq atneuc ne agneT .selbalacse adbmal salger ed sonimr©Ât ne nad es n³Ãicaunitnoc a o±Ãesid ed salger saL .soirotaela osecorp ed senoicairav sal a odibed ojab s¡Ãm aes otneimidner le euq arepse es orep ,lanoicnuf pihc nu odatluser omoc rad edeup n⁰Âa o±Ãesid led o±Ãesid ed salger sal ed sanugla aloiv euq o±Ãesid nU .n³Ãicairbaf ed etol nu ed selbatpeca spihc ed n³Ãicaler atreic anu ,riced se ,odanimret otcudorp le arap otneimidner otreic nu razitnarag arap salger satse riuges ebed o±Ãesid ed roda±Ãesid lE .n³Ãicairbaf ed osecorp le y aÃgoloncet al rop aracs¡Ãm ed sapac sal a satseupmi sacirt©Ãmoeg senoiccirtser sal natcid euq ,o±Ãesid ed o±Ãesid ed salger ed otnujnoc nu a esratsuja ebed aracs¡Ãm ed o±Ãesid ed o±Ãesid adac ,2 olutÃpaC le ne ³Ãitucsid es ay omoC SOMC o±Ãesid ed o±Ãesid ed salgeR 2.3 .1.3 arugif al ne artseum es ovitareti osecorp etse ed ojulf ed amargaid lE .atis¡Ãrap al ricuder arap otiucric led aÃgolopot al adot o sazeiP sol sol .ominÃm o±Ãamat ed serotsisnart noc rosrevni le ra±Ãesid somatnetni euq agnopuS .o±Ãesid ed salger sal noc odreuca ed selaudividni serotsisnart sol raerc somatisecen ,oremirP .elpmis yum otiucric etse arap osulcni setnerefid The active urene is then determined by the minimum difference of diffusion contact (which is necessary for connections of origin and drainage) and the minimum separation of the diffusion contact in both active Érus edges. The width of the polysilicium with the active ã¡rea (which is the door of the transistor) is taken as the width of the polythy (Fig. 3.3). Then, the total active length is simply determined by the following sum: (Poly width) + 2 x (mint spacing of contact polyes) + 2 x (spacing minimum from contact to the edge of the edge of Active core). The PMOS transistor must be placed in a n-well-well region, and the minimum size of the well is dictated by the active pee of pmos and the minimum overlapping of n-bee on n+. The distance between the NMOS and the PMOS transistor is determined by the minimum separation between the active n+ and the N-Bien (Fig. 3.4). The polysilic doors of the NM and the transistors of PMOS are generally aligned. The final step in the designer of the Mã¡scara is the local interconnections in metal, for the output node and for the VDD and GND contacts (Fig. 3.5). Keep in mind that to be biased correctly, the N-Well region must also have a contact with VDD. Figure 3.3: Restrictions of design rules that determine the dimensions of a minimum size transistor. Figure 3.4: Placement of a NMOS and a PMOS transistor. Figure 3.5: Complete minor design of the CMOS inverter. The initial phase of the design design can be significantly simplified by using stick diagrams, or the so -called symbolic design. Here, the detailed design design rules are simply neglected and the main characteristics (active areas, polysilicio, metal lines) are represented by constant rectals or simple stalls or simple sticks. The proposal of the stick diagram is to provide the .otelpmoc .otelpmoc aracs¡Ãm ed amargaid nu rajubid nis omitp³Ã o±Ãesid le arap sedadilibisop sairav etnemadip¡Ãr raborp y sacig³Ãlopot senoicatimil sal ed n³Ãisnerpmoc aneub anu ed aer¡Ã le y SOMP serotsisnart sol arap P opit ed n³Ãisufid ed aer¡Ã le ,ÃuqA .apac alos anu ed latem y apac alos anu ed oicilisilop odnazilitu ,sadartne sod ed DNAN atreup anu y RON sadartne sod ed atreup anu ed artseum ed so±Ãesid sol artseum 7.3 arugiF aL .SOMC rosrevni led o±Ãesid le arap etnemroiretna sodanimaxe selareneg soipicnirp sol neugis SETAG RON y DNAN SOMC ed aracs¡Ãm al ed o±Ãesid ed so±Ãesid soL setaG roN y dnaN SOMC ed o±ÃesiD 4.3 .SOMC rosrevni led o±Ãesid ed senoicpo sairav nartseum euq olap ed samargaiD :6.3 arugiF .roirepus etrap al ne sela±Ães sert raturne arap azilitu es euq ,latem ed apac arecret anu rasu ed dadilibisop anu artseum 6.3 .giF al ne lanif o±Ãesid ed olpmeje lE .adilas ed sela±Ães sal y adartne al etnemlacitrev rata arap rasu edeup es ,etnemavitanretla o ,arreit y aicnetop ed ortsinimus ed saenÃl arap rasu edeup es levin odnuges ed latem lE .n³Ãixenocretni ed datrebil s¡Ãm etimrep latem ed apac adnuges anu ed n³Ãicida aL .rasap nedeup euq latnoziroh latem ed saenÃl sal a setnerapsnart serosrevni sol ed serotsisnart sol euq ecah otsE .arreit ed senoixenoc sal y aicnetop al rednetxe arap esrasu nedeup serotsisnart sobma ed n³Ãisufid ed saer¡Ã sal ,etnemavitanretlA .rosrevni led s©Ãvart a nasap euq sela±Ães sal raturne arap rasu edeup es aroha 1-lateM . 2-latem ed lacitrev aenÃl ana a natcenoc es zev us a euq ,serotsisnart sol ed ejanerd ed selanimret sol a redecca arap latnoziroh latem ed saerroc rasu nedeup es ,ahcered a adreiuqzi ed adlec al ed oidem led s©Ãvart a latem ed saenÃl sod o anu rasap nebed es is ,olpmeje roP .rosrevni le erbos sadaturne res nebed sela±Ães sarto ,sosac sonugla nE .serotsisnart sol ed senoicaenila setnerefid noc ,sacis¡Ãb s¡Ãm rosrevni ed senoicarugifnoc sod sal nos 6.3 .giF al ne nartseum es euq olap ed amargaid ed so±Ãesid sod soremirp soL .SOMC rosrevni otiucric le arap o±Ãesid ed senoicpo setnerefid nartseum euq olap ed samargaid ed eires anu someranimaxe ,n³Ãicaunitnoc A type N for NMOS transistors are aligned in parallel to allow a simple routing of door signals with two parallel polysilicio lines running vertically. Also note that the two mask designs show a very strong symmetry, due to the fact that the ed orem⁰Ãn le raziminim somedop iS .lanoicida oicilis ed aer¡Ã ed elbaredisnoc daditnac anu emusnoc etnematreic otsE .n³Ãisufid-n³Ãisufid ed n³Ãicarapes anu y sodal sobma ne acil¡Ãtem n³Ãisufid ed sotcatnoc sod ritimrep arap omoc ailpma etnemetneicifus ol res ebed nocilisyloP ed sanmuloc sal ertne n³Ãicarapes al ,osac etse ne euq atneuc ne agneT .nocilisyloP atreup al ed sanmuloc sal ed oirartibra nedro nu odnazilitu ,½Às'tpmettA" nu ed olap ed amargaid ed o±Ãesid le artseum 11.3 arugiF aL .SOMC acig³Ãl ed atreup ajelpmoc al arap aminÃm aer¡Ã ed o±Ãesid nu riurtsnoc ed amelborp le someragitsevni ,arohA .adartne ed selbairav 5 noc anaeloob n³Ãicnuf anu azilaer euq SOMC ed acig³Ãl ed atreup ajelpmoc anu :01.3 arugiF .ofirg elbod ed otpecnoc le odnazilitu etnemlic¡Ãf riurtsnoc edeup es SOMP serotsisnart ed pu-llup der al ,SOMN ed n³Ãiccartxe ed der al ed der al ed aÃgolopot al econoc es euq zev anU .SOMC acig³Ãl atreup ajelpmoc anu ed setneidnopserroc der ed socif¡Ãrg sol y otiucric ed amargaid le artseum 01.3 arugiF aL .pu-llup ed der al neyutitsnoc euq SOMP ed serotsisnarT etneidnopserroc eires al ed etneidnopserroc laud der anu y elbagelpsed der adamall al neyutitsnoc euq SOMN serotsisnart ed eires ne alelarap der anu ereiuqer etnemlareneg)otcudorp led sonimr©Ât soirav y adartne ed selbairav sairav riulcni nedeup euq(sajelpmoc sanaeloob senoicnuf ed n³Ãicazilaer aL SOMc ed sojelpmoc sojelpmoc 5.3 .2DNAN SOMC atreup anu ed aracs¡Ãm ed o±Ãesid le rareneg arap soirasecen selapicnirp sosaP :9.3 arugiF .2RON SOMC atreup anu ed aracs¡Ãm ed o±Ãesid le rareneg arap soirasecen selapicnirp sosaP :8.3 arugiF .2DNAN SOMC atreup anu y 2RON SOMC atreup anu ed artseum ed so±ÃesiD :7.3 arugiF .aracs¡Ãm ed sapac sal etnemavisergorp odneinifed y olap ed amargaid le edsed odnaznemoc ,satreup sabma arap aracs¡Ãm ed o±Ãesid ed o±Ãesid led selapicnirp sosap sol nartseum 9.3 y 8.3 sarugif sal ,etnemlaniF .ocirt©Ãmis otiucric led aÃgolopot anu eneit RON atreup al y active area for both the NMOs and PMOS transistors, the separation between the columns of the Polysilicon door can be made smaller. This, in turn, will reduce the overall horizontal dimension and the general area of circuit design. Number saÃv rartnocne se aigetartse rojem al ,osac ese nE .pu-llup der al ne omoc elbagelpsed der al ne otnat atelpmoc reluE atur anu riurtsnoc elbisop aes erpmeis on euq elbisop sE .SOMC acig³Ãl atreup ajelpmoc al ed odazimitpo olap ed amargaid ed o±ÃesiD :31.3 arugiF .a±Ãeuqep s¡Ãm airatisarap aicnaticapac al ,aicneucesnoc ne ,y sela±Ães sal ed elpmis otneimaturne le ,)a±Ãeuqep s¡Ãm(atcapmoc s¡Ãm o±Ãesid ed aer¡Ã le nos o±Ãesid oveun etse ed sajatnev saL .latem ed n³Ãisufid ed otcatnoc nu olos ritimrep ebed sanicev ilop ed sanmuloc sod ertne n³Ãicarapes al ,osac etse nE .31.3 arugif al ne artseum es o±Ãesid oveun led olap ed amargaid lE .OMP serotsisnart arap y OMN arap sadipmurretnini savitca saer¡Ã odatluser omoc ad euq ol ,aicneuces atse noc odreuca ed razinagro nedeup es etaG nocilisyloP ed sanmuloc saL .socif¡Ãrg sobma ne)C-B-A-D-E(nº Ãmoc aicneuces anu yah euq ev eS .)y(ne animret y)x(ne azneimoc reluE atur al ,sosac sobma nE .avitca aer¡Ã ed sosnacsed ed orem⁰Ãn le aziminim euq atreup ed nedro nu anoicroporp pu-llup y elbagelpsed der al arap socif¡Ãrg sobma ne n⁰Ãmoc reluE atur anu rartnocnE :21.3 arugiF .olpmeje ortseun ne socif¡Ãrg sobma arap n⁰Ãmoc reluE atur anu ed n³Ãiccurtsnoc al artseum 21.3 arugiF aL .zev anu etnematcaxe acif¡Ãrg al ed)amar(edrob adac aseivarta euq adipmurretnini atur anu omoc enifed es reluE atur aL .socif¡Ãrg sobma arap n⁰Ãmoc relue atur anU rartnocne ,riced se ,adartne ed sateuqite sal ed ocitn©Ãdi odidep le noc pu-llup der ed ocif¡Ãrg le ne reluE ed atur anu y elbagelpsed der ed ocif¡Ãrg le ne reluE atur anu rartnocne etnemelpmis :htaP-reluE odot©Ãm le se amitp³Ã atreupmoc ed nedro le rartnocne arap elpmis odot©Ãm nU .nocilisyloP ed atreup al ed sanmuloc sal ed oirartibra nedro nu noc ,SOMC acig³Ãl atreup ajelpmoc al ed olap ed amargaid led o±ÃesiD :11.3 arugiF .serotsisnart sol ed nedro le odnaibmac ,riced se ,oicilisilop ed sanmuloc sal ed nedro le odnaibmac raziminim nedeup es avitca aer¡Ã ed sarutpur saL in both graphics, which should be as long as possible. This approach tries to maximize the number of transistors that can be placed in a single, uninterrupted active area.Fig. 3.14 shows the circuit diagram of a staircase full of a single bit CMOS. The circuit has three inputs, and two outputs, sum and port_out. The corresponding mask design of this circuit is given in the Fig. 3.15. All input and output signals have been arranged in vertical polysilicon columns. Note that both the sum circuit and the load circuit have been performed using an active area uninterrupted each. Figure-3.14: Circuit scale of the staircase filled with a single bit CMOS. Figure-3.15: Provision of full-circuit CMOS ladder masks. This chapter edited by Y. Leblebici a joint production of KGF
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